

A Slave CDP1802 Serial Printer Buffer System

by K. Nagy

This Note describes a CDP1802-based stand-alone line-printer buffer that links a master processor system to a serial printer through an RS-232C interface. The main buffer board consists of a CDP1802 Microprocessor (configured as a peripheral controller), a CDP1854A UART with baud-rate generation devices (configured in Industry mode 0 and able to handle separate receive and transmit baud rates), and a CDP18U42 EPROM (to store a minimal user program). With the addition of RCA Microboards for system RAM (CDP18S620, CDP18S621, CDP18S622, CDP18S623, CDP18S624, or CDP18S625 in various configurations from 4K to 16K), a buffer system with a printer character storage capacity of up to 32K bytes can be implemented.

The line buffer is especially useful with interactive computer systems; it frees high-speed terminals for other tasks while a slower printer (connected in parallel to the terminal through a serial port, such as is used with RCA Development Systems) prints from buffer memory. The buffer circuitry also illustrates how a CDP1800 processor can be configured as a slave controller that communicates with a master system through a serial port. In this configuration, some of the special I/O features of CDP1800 architecture are highlighted; these features include DMA control for high-speed data transfer, I/O instructions for communication with peripheral chips such as the CDP1854A UART, and the availability of several input flag lines for event polling.

The low power consumption of the system makes it ideal for operation from a storage battery, which provides portability of user data, and also protects data integrity should a line power failure occur.

System Modes

The line buffer operates in the following modes:

1. Receive data—The print buffer is loaded at some (usually high) baud rate (through a serial interface under CDP1802 DMA control).
2. Transmit data—Data is transmitted, usually at a low baud rate (through a serial interface under CDP1802 programmed I/O control), to the printer when the printer is selected and ready.
3. Instant replay—Data is retransmitted to the printer upon request.

These modes permit the system to accommodate a wide range of input and output conditions, and to communicate with many different peripheral devices.

System Set Up

The line-buffer system input and output is connected to suitable sending and receiving units equipped with RS-232C interfaces by means of cables and connectors. The

system output contains a feedback (handshake) line that permits the printer to operate at its optimum speed; the feedback feature can be eliminated if necessary through software changes.

The printer-buffer prototype was evaluated using a CDP18S007 CDS Development System, an ADM-3A CRT Terminal, and an EPSON MX-80 Printer. However, the universal nature of the buffer design permits it to be used with a wide variety of master system and printer combinations.

Hardware

A block diagram of the system is shown in Fig. 1; detailed system Interconnection diagrams are shown in Appendix A. The "U" designators used in the following text refer to the figures in Appendix A, and are identified in Table I and in the Appendix. Table II summarizes register assignments.

Table I — List of IC's Used in System

IC	Identity
U1	CDP1802 CPU
U2	CDP18U42 EPROM
U3	CDP1854A UART
U4	CD4013 D FF
U5, U6	CD4069 Hex Inverter
U7	CD4093 Quad 2-Input NAND
U8	CD4013 D FF
U9, U10, U11	CD40161 Sync Binary Counter
U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

Table II — Line-Buffer Register Use

R0	Initial Program Counter/DMA-IN Pointer
R3	Program Counter
R4	Printer Pointer
R5	End of Memory Pointer
R6	XOR Temporary Location Pointer
R7	Temporary DMA-IN Pointer
R8	Cold Start Flag

The system program resides in the CDP18U42, 256-byte UV Erasable PROM, U2, located in the lower 32K address space on the system map. The chip-select signal for the EPROM is generated by latching the high-order address byte of the MA7 signal by means of a CD4013 flip-flop (U4). The EPROM is selected when MA.1 is low (CS1), MRD is low (CS3), and CLR is high (CS2).

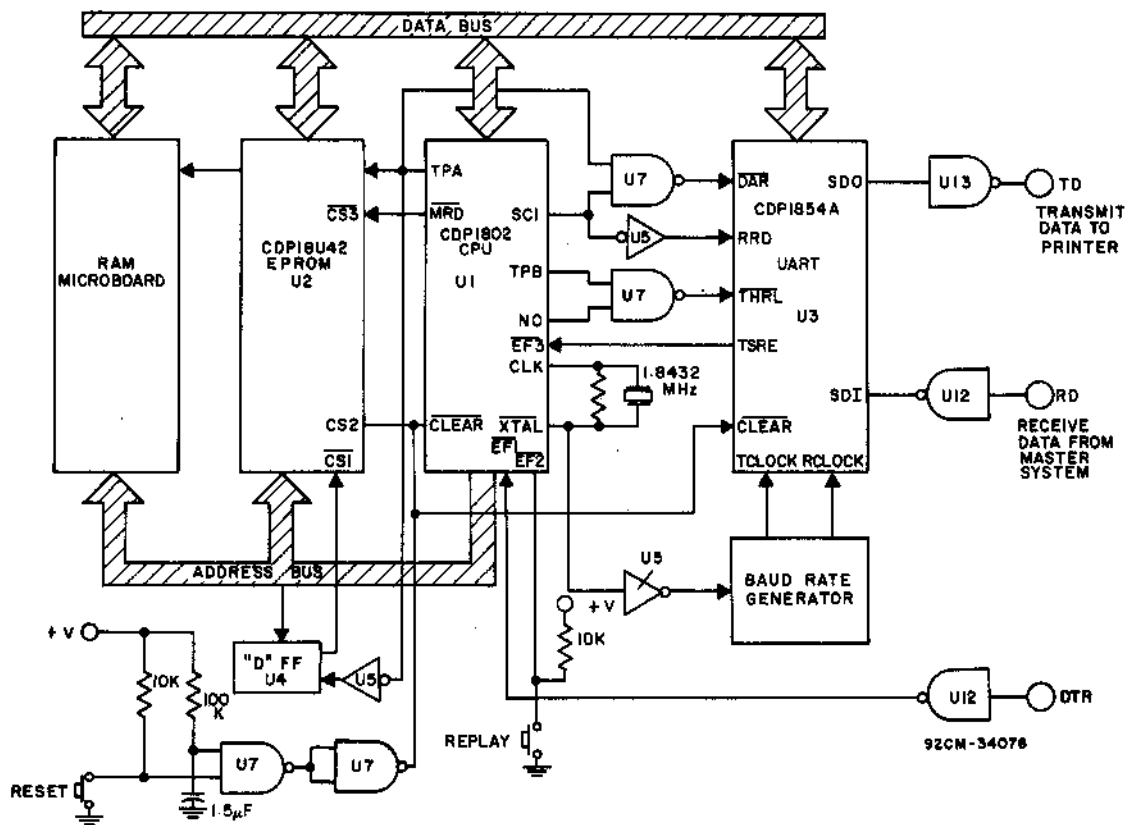


Fig. 1 - Block diagram of the serial printer buffer system.

The internal oscillator of the GDP1802 microprocessor is driven by a 1.8432-MHz external crystal, which acts as the system master clock. The crystal is connected between the CLOCK and XTAL terminals of the microprocessor. One inverter of the CD4069 (U5) provides a buffered signal called CLK OUT to the baud-rate generator divider chain for the UART.

Part of a CD4093 (U7) forms a power-on reset circuit that outputs a CLEAR signal to the microprocessor and the UART. An external reset signal can force the processor to restart program execution. An SPST switch connected to the EF2 flag-input terminal of the microprocessor provides the instant-replay request signal for the program. If this switch is in the replay mode, activation of the reset button will start the printing of the previously deposited contents of the RAM buffer. This feature relieves the host computer of the time-consuming task of producing copies on the printer.

A CDP4013, Dual D Flip-Flop (U8), forms a synchronous divide-by-three circuit; its output is connected to two CD40161B cascaded synchronous binary counters (U9 and U10). The Q outputs of U9 and U10 provide baud rates from 150 to 19,200 baud. The accuracy of these baud rates is comparable to that of the crystal oscillator. Another CD40161B synchronous binary counter (U11) is used in a divide by 11 configuration to generate the 110 baud used by some teletypes and other slow mechanical printers. Because it is possible to input to, or output from, this system at varying baud rates, the system is very useful in interactive applications or where baud-rate exchange is required.

The CDP1854A UART (U3) has two modes of operation. Mode 1 is directly compatible with the CDP1800 family of microprocessors without additional interface circuitry; software techniques are used for programming in this

mode.¹ In Mode 0, the mode used in the serial printer buffer system, the CDP1854A is compatible with a great many other UART's, such as the TR1602A by Western Digital, and provides the user with hardware-option selection in the form of five independent switches. The functions of the switches are as follows:

- SW5- When open, the generation of parity is inhibited.
- SW6- When open, two stop bits are selected, when closed, one is selected. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.
- SW7, SW8- These two switches select the character length (exclusive of parity) of five to eight data bits.
- SW9- This switch is closed for odd parity, opened for even parity.

Fig. 2 shows serial-word format-programming data. The UART has two independent byte-wide buses. Both receive and transmit buses are connected to the system data bus.

The system receive operation is initiated when a serial bit stream is sent via the RS-232 receiver interface to the UART. When the UART receiver assembles a full received character, the data available (DA) output goes high and initiates a DMA-IN cycle. During DMA, the CPU is forced into a DMA cycle (S2), which causes SC1 to go high; the result is a transfer of data from the UART receiver holding register to the data bus. The address and control signals needed to direct the flow of data into the RAM pointed to by DMA pointer R0 are generated during DMA. Additionally, hardware interconnections are made that cause the data available reset (DAR) flag to be reset. Reset is accomplished through a signal to the data available reset (DAR) input; the signal terminates the DMA-IN request before it is again sampled by the CPU. Finally, R0 is incremented at the end of the S2 cycle, and the system is ready for transfer of another byte of data when it is received.

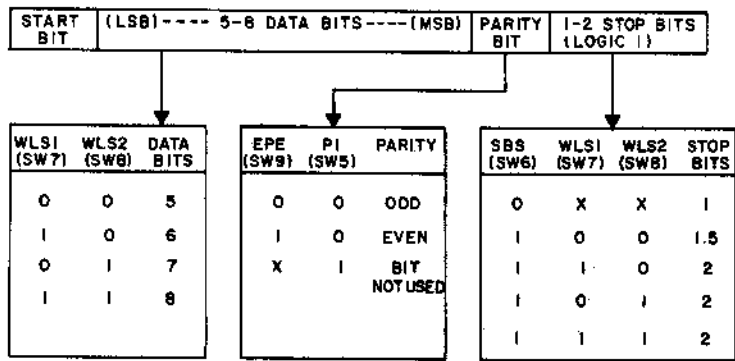


Fig. 2 - Description of serial word format programming.

The system transmit operation begins when the UART transmitter shift register is empty (TSRE high, polled via EF3) and the printer is selected (polled via EF1). The CPU issues an I/O command that signals the transmitter holding register load (THRL) input to transfer data from the data bus to the transmitter holding register. The data is serialized by the transmitter shift register and output, in the format selected by the user, through the serial data out (SDO) line and the RS-232 line driver to the printer. During the time that data is actively being transmitted by the UART, the TSRE signal will be low, preventing transmission of additional data. When the TSRE signal becomes high, and the printer is ready, a character can be transferred from the system data bus to the transmitter holding register. The microprocessor then outputs a low pulse to the UART transmitter holding register load (THRL) input, causing TSRE to go low. When the TSRE output signal goes high again, and EF1 is low (indicating that the printer is ready), another character can be loaded into the transmitter holding register for transmission. This process is repeated until all of the line-buffer memory contents are transmitted.

Baud-Rate Generation

The CDP1854A UART requires a clock signal that is 16 times the desired bit rate for proper operation. This 16X clock rate is applied to the UART receive clock (RCLOCK) and transmitter clock (TCLOCK) inputs. In the subject system, the RCLOCK and TCLOCK inputs are connected to separate frequencies (through SW 3 and SW 4). Both of these bit rates are derived from the same crystal oscillator and divider circuitry.

The bit rate and the number of bits per character determine the number of characters that can be transmitted in one second. If the UART receiver is required to operate at a data rate of 19,200 bits/s, then the receive clock (RCLOCK) frequency must be $16 \times 19,200 = 307,200$ Hz. Consequently, if the data transmission rate must be 300 bits/s, then the TCLOCK input of the UART must be connected to a clock frequency of $16 \times 300 = 4800$ Hz. Table III shows baud rates and frequencies supported by the system.

Software

The program flowchart is shown in Fig. 3. Upon power-on,

Table III - Baud Rates and Frequencies Supported by System

Baud Rate	16X Freq. (kHz)	Time (μs)
110	1.760	568.18
150	2.400	416.67
300	4.800	208.33
600	9.600	104.17
1200	19.200	52.08
2400	38.400	26.04
4800	76.800	13.02
9600	153.600	6.51
19200	307.200	3.26

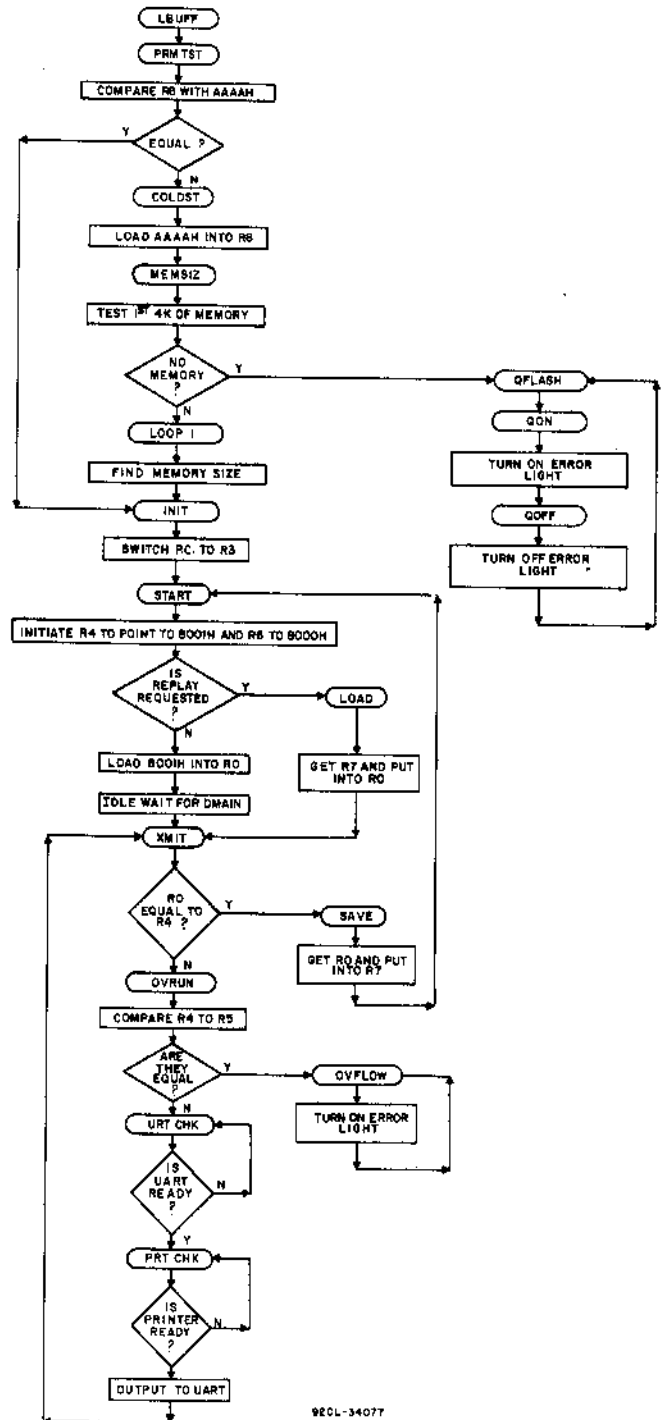


Fig. 3 - Program flowchart.

the power-on reset circuit initiates program execution from the first ROM location (located at 0000). After program execution has begun, the first part of the program, PRMTST, tests register R8 to determine if a "cold" or first start is being initiated. If the start is not a first start, then R8 contains AAAAH, which results in the execution of the routine INIT. If a cold start is encountered, R8.1 and R8.0 will contain random values, and the program will branch to the cold-start routine COLDST. This routine sets R8 to AAAAH, and passes control to the memory-size test routine, MEMSIZ, which determines the amount of RAM available in the system for line-buffer use. If there is no RAM connected to the system, the QFLASH routine is entered, and the error LED flashes on and off until the condition is corrected and the reset button pressed. Upon completion of the memory-size routine, register R5 will contain the size of the user RAM. The system then undergoes initialization under software control through execution of the routine INIT.

The INIT routine initializes the printer pointer and DMA pointer to 8001H (the first available RAM location) and the program counter to R3. A byte of RAM is set aside at location 8000H for use by the program. When initialization is complete, the program checks for the instant-replay request ($\overline{EF2}$ low); if it finds no request, it goes to idle and waits for the first byte received by the UART receiver to initiate a DMA-IN.

As the processor receives a DMA-IN request, it places the byte, now on the data bus, in the location pointed to by DMA pointer R0. When the DMA cycle is completed, the processing of the XMIT routine begins by comparing the DMA pointer (R0) to the printer pointer (R4). If these two pointers are not set to the same location in memory, the XMIT routine determines whether the printer pointer is set to an address within the valid boundaries of the memory buffer. If it is not, an error is indicated by an error light; if it is, program control is passed to the UART checking routine, URTCHK.

The URTCHK routine first checks the UART transmitter-shift-register-empty signal, TSRE. If TSRE is high, control goes to the printer checking routine, PRTCHK. When this routine receives a ready signal from the printer, it outputs a character to the printer through the transmitter side of the UART. After the byte has been transferred to the UART transmitter holding register, the system proceeds with the XMIT routine until the entire contents of the buffer are printed out.

In the subject system, all incoming data is deposited in memory in real time by DMA-IN within an execution time of one CPU machine cycle per byte. This method is similar but superior to that of an interrupt driven system because it does not have the overhead associated with the interrupt software routine and, therefore, can easily cope with high incoming baud rates.

At baud rates of 19,200 bits per second and 10 bits per character, the system has approximately 520 microseconds of time available for processing between two successive DMA-IN pulses. At a system clock rate of 1.8432 MHz (selected for the baud-rate generation circuits for the UART), the system has enough time to execute approximately 120 machine cycles before the next DMA-IN cycle comes in.

The software assembly listing in ASM 4 is shown in Appendix B.

Summary

In summary, this system is especially useful in applications requiring interaction with a variety of types of equipment as it is capable of taking input or providing output at varying baud rates. The instant-replay feature relieves a host computer of the time consuming task of producing copies on a printer. The system UART, when used in mode 0, constitutes a peripheral device that makes interfacing of the line-buffer system with other systems a simple matter. The low power consumption of the line-buffer system makes it an ideal one for operation from a storage battery, which provides portability of user data and protection of this data in the event of a line-power failure.

References and Bibliography

1. "Use of the CDP1854 UART with RCA Microprocessor Evaluation Kit CDP18S020 or EK/Assembler-Editor Design Kit CDP18S034," R.G. Ott, RCA Solid State Application Note ICAN-6632.
2. "COS/MOS Memories, Microprocessors, and Support Systems," RCA Solid State Databook SSD-260.
3. "COS/MOS Integrated Circuits," RCA Solid State Databook SSD-250.
4. "COS/MOS Integrated Circuits Manual," RCA Solid State publication CMS-272.
5. "User Manual for the CDP1802 COSMAC Microprocessor," RCA Solid State publication MPM-201.

Appendix A

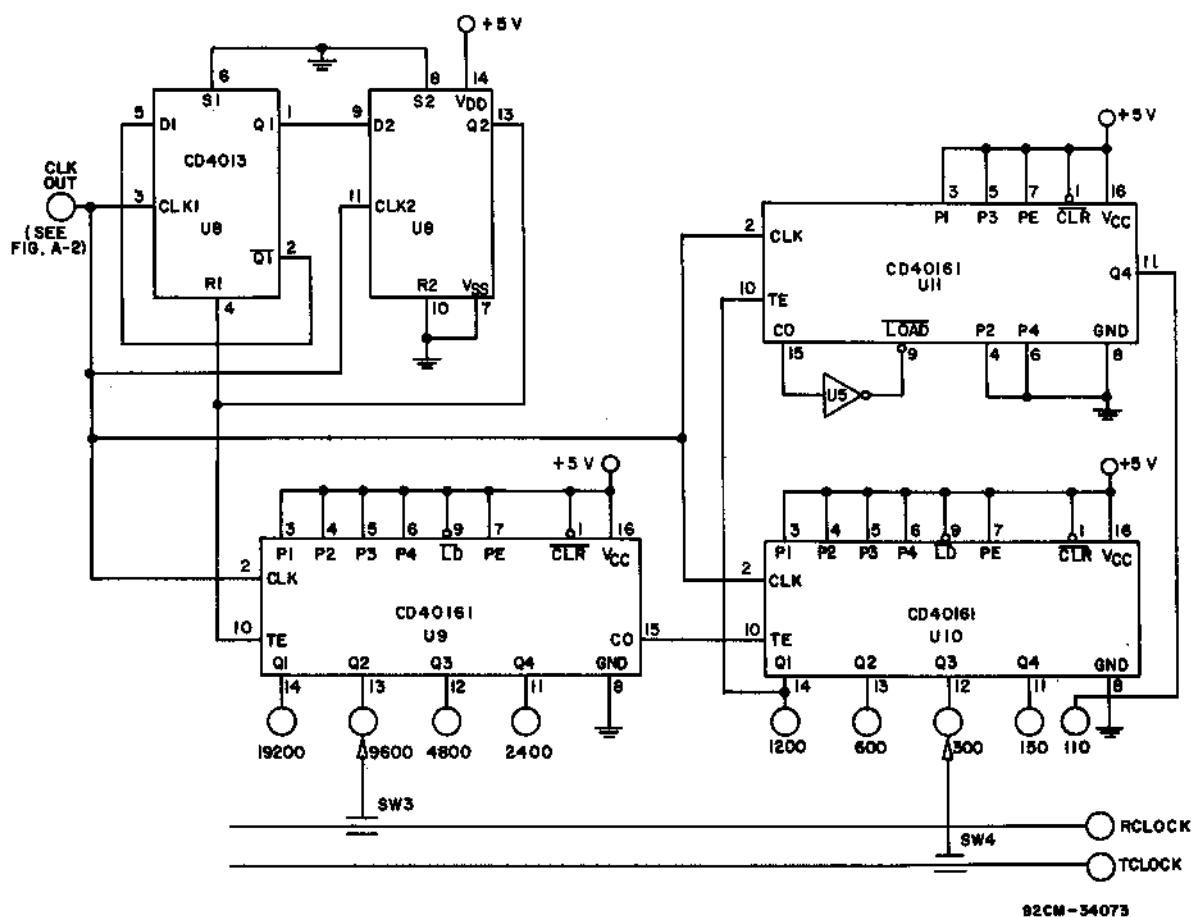


Fig. A-1 - Interconnection diagram for line-buffer baud-rate generator.

Table A-I - Microboard Computer Bus Interface (Fig. A-2)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMA1-N
B	TPB-P	2	DMA0-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	-5 V/-15 V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12 V/+15 V
Y	+5 V	21	+5 V
Z	GND	22	GND

Table A-II - List of IC's Used in System

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U1	CDP1802 CPU
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U8	CD4013 D FF
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U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

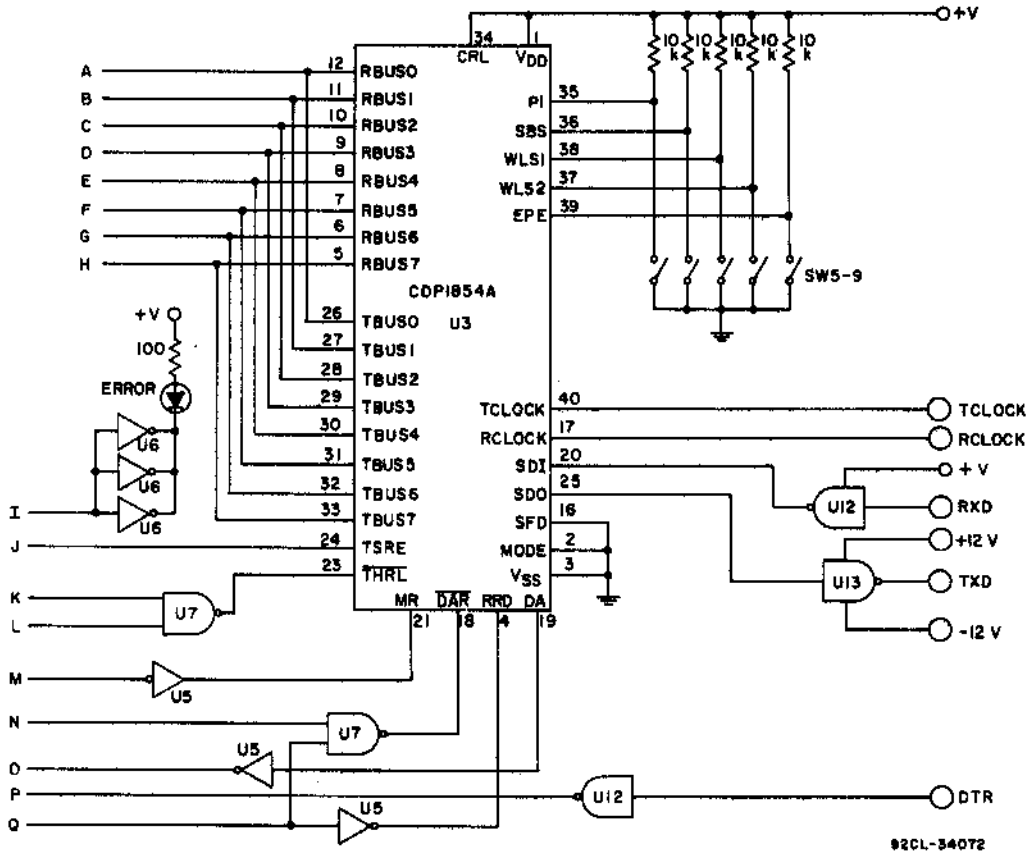


Fig. A-3 - Interconnection diagram for line-buffer receiver/transmitter.
 (Letters A through Q on left match this figure with Fig. A-2 on facing page.)

Appendix B (Cont'd)

0019 B5;	0026 PHI R5	.. IN THE SYSTEM MIN. 4K.
001A FBFF;	0027 LDI #FF	.. MAX. 32K.
001C A5;	0028 PLO R5	
001D E5;	0029 SEX R5	
001E FBAA;	0030 LDI #AA	
0020 55;	0031 STR R5	
0021 F5;	0032 SD	
0022 3236;	0033 BZ LOOP1	
0024 7B;	0034 QFLASH: SEQ	.. IF SYSTEM MEMORY IS
0025 FB20;	0035 LDI #20	.. LESS THAN 4K FLASH
0027 B5;	0036 PHI R5	.. ERROR LITE
0028 25;	0037 QON: DEC R5	
0029 95;	0038 GHI R5	
002A 3A2B;	0039 BNZ QON	
002C 7A;	0040 REQ	
002D FB20;	0041 LDI #20	
002F B5;	0042 PHI R5	
0030 25;	0043 QOFF: DEC R5	
0031 95;	0044 GHI R5	
0032 3A30;	0045 BNZ QOFF	
0034 3024;	0046 BR QFLASH	
0036 95;	0047 LOOP1: GHI R5	
0037 FC10;	0048 ADI #10	
0039 B5;	0049 PHI R5	
003A FBAA;	0050 LDI #AA	

Appendix B (Cont'd)

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003C 55;          0051          STR R5
003D F5;          0052          SD
003E 3236;       0053          BZ LOOP1
0040 95;          0054          GHI R5
0041 FF10;       0055          SMI #10
0043 B5;          0056          PHI R5          ..R5=MEMORY SIZE
0044 F800;       0057 INIT:      LDI #00
0046 B3;          0058          PHI R3          ..SWITCH PC TO R3
0047 A6;          0059          PLO R6
0048 F84C;       0060          LDI A.0 (START)
004A A3;          0061          PLO R3
004B D3;          0062          SEP R3
004C F8B0;       0063 START:     LDI #80          ..INIT.PRINTER POINTER - R4
004E B6;          0064          PHI R6          ..TO BEGINNING OF RAM; 8001H
004F B4;          0065          PHI R4          ..AND XOR TEMPORARY HOLDING
0050 F801;       0066          LDI #01          ..LOCATION - R6 TO 8000H
0052 A4;          0067          PLD R4
0053 3583;       0068          B2 LOAD          ..CHECK FOR INSTANT REPLAY
0055 A0;          0069          PLO R0          ..REQUEST. REPLAY IF 0
0056 F8B0;       0070          LDI #80
0058 B0;          0071          PHI R0          ..INITIALIZE DMA POINTER - R0
0059 F800;       0072          LDI #00          ..TO 8001H
005B 00;          0073          IDL
005C E6;          0074 XMIT:      SEX R6          ..ALL INPUT PRINTED?
005D 94;          0075          GHI R4
005E 56;          0076          STR R6
005F 90;          0077          GHI R0
0060 F3;          0078          XOR
0061 3A69;       0079          BNZ OVRUN
0063 B4;          0080          GLO R4
0064 56;          0081          STR R6
0065 B0;          0082          GLO R0
0066 F3;          0083          XOR
0067 327D;       0084          BZ SAVE
0069 93;          0085 OVRUN:     GHI R5          ..OVER-RUN TEST ON
006A 56;          0086          STR R6          ..PRINT BUFFER
006B 94;          0087          GHI R4
006C F3;          0088          XOR
006D 3A75;       0089          BNZ URTCHK
006F B5;          0090          GLO R5
0070 56;          0091          STR R6
0071 B4;          0092          GLO R4
0072 F3;          0093          XOR
0073 32BF;       0094          BZ OVFLOW
0075 3675;       0095 URTCHK:     B3 URTCHK          ..WAIT FOR UART READY
0077 3C77;       0096 PRTCHK:     BN1 PRTCHK          ..PRINTER READY TEST
0079 E4;          0097          SEX R4          ..READY IF HI
007A 61;          0098          OUT 1
007B 305C;       0099          BR XMIT
007D 90;          0100 SAVE:      GHI R0
007E B7;          0101          PHI R7
007F B0;          0102          GLO R0
0080 A7;          0103          PLO R7
0081 304C;       0104          BR START
0083 97;          0105 LOAD:      GHI R7
0084 B0;          0106          PHI R0
0085 B7;          0107          GLO R7
0086 A0;          0108          PLO R0
0087 305C;       0109          BR XMIT
0089 FBAA;       0110 COLDST:    LDI #AA
008B B8;          0111          PHI R8
008C AB;          0112          PLO R8
008D 3017;       0113          BR MEMBIZ
008F 7B;          0114 OVFLOW:    SEQ          ..PRINT LENGTH EXCEEDED AMOUNT
0090 30BF;       0115          BR OVFLOW          ..OF AVAILABLE RAM IN SYSTEM.
0092 ;           0116          END          ..ERROR LITE IS ON STEADY.
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